Sony's 25 nano sec access time world-fastest 4MSRAM CMOS chip became the basic process for Sony modern CMOS image sensors

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A 25-ns 4-Mbit CMOS SRAM with Dynamic Bit-Line Loads

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Abstract — A 25-ns 4-Mbit CMOS SRAM with 512K word × 8-bit organization has been developed. The RAM was fabricated using a 0.5-μm double-poly and double-aluminum CMOS technology and was assembled in a 32-pin 400-mil DIP. A small cell size of 3.6 × 5.875 μm^2 and a chip size of 7.46 × 17.41 mm^2 were obtained. A fast address access time of 25 ns with a single 3.3-V supply voltage has been achieved using our newly developed dynamic bit-line load (DBL) circuit scheme incorporated with an address transition detector (ATD), divided word-line structure (DWL), three-stage sense amplifier, and low-noise output circuit approach. A low operating current of 46 mA at 40 MHz and low standby currents of 70 μA (TTL) and 5 μA (CMOS) were also attained.

I. Introduction

THE MEMORY capacity of SRAM's has quadrupled every two or three years due to recent advances in circuit, device, and process technology. In addition, SRAM's have achieved a higher performance in terms of their fast access time and low standby current. The low standby current is required for battery backup applications, e.g., hand-held computers, RAM cards, electronic still cameras, and printers, etc. The faster access time is also needed for the fields of main memory in supercomputers, cache/buffer memory in minicomputers, workstations, and test pattern memory in VLSI test systems. Several medium-speed 1-Mbit CMOS SRAM's with byte-wide organization for these purposes have already been reported [1]–[4].

This paper will describe a byte-wide organization 4-Mbit CMOS SRAM with a typical address access time of 25 ns and a single 3.3-V supply voltage [5]. This RAM was fabricated using a 0.5-μm double-polysilicon and double-aluminum CMOS technology. JEDEC has proposed a power supply voltage of 3.3 V for future chips, so we adopted this voltage in our prototype 4-Mbit CMOS SRAM. This power supply voltage of 3.3 V has made possible a highly reliable 0.5-μm level CMOS VLSI with low power dissipation and high-speed operations. A 25-ns address access time was achieved by our newly developed dynamic bit-line load (DBL) circuit scheme incorporated with an address transition detector (ATD), divided word-line structure (DWL), three-stage sense amplifier [6], [7] and low-noise output circuit approach.

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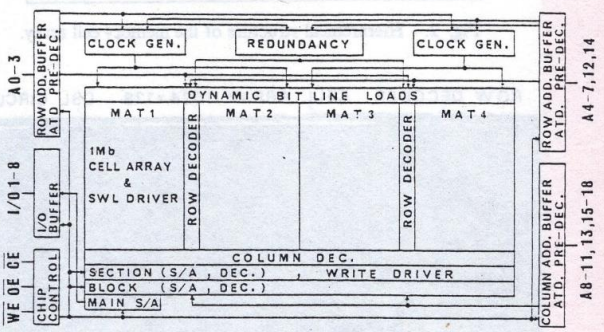

Fig. 1. Block diagram of the RAM.

In Section II, circuit technologies, which include the chip architecture, the DBL circuit, the sense amplifier, and the low-noise output circuit, will be described. In Section III, the process technology will be explained. The performance of the RAM and conclusions are given in Sections IV and V, respectively.

II. Circuit Design

In order to achieve a fast access time, three factors had to be considered: a) how to reduce the signal delay time of the word line, b) how to amplify the memory cell data and transmit it quickly to the output circuit, and c) how to reduce the noise caused by the output circuit. In the following sections, new chip architecture and circuit techniques to realize these three factors are described.

A. Chip Architecture

In order to minimize the signal delay time, the optimum allocation of the peripheral circuit and the compact layout design were considered. A block diagram of the RAM is shown in Fig. 1. The hierarchical structure of a memory cell array with the 512K word × 8-bit organization is shown in Fig. 2. The address signals are divided into two groups: row and column. The column address signals are used for

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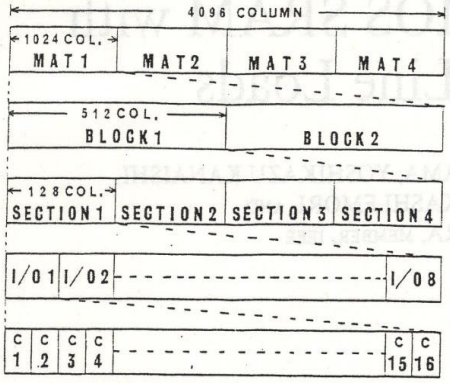

Fig. 2. Hierarchical structure of the memory cell array.

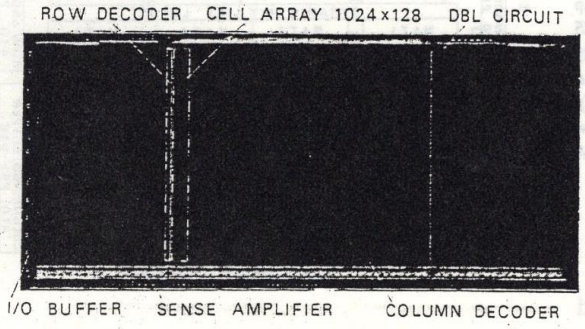

Fig. 3. Photomicrograph of the chip.

column selection, block selection, and mat selection. Each address input buffer has a local ATD pulse generator. A detection signal from any of the local ATD-pulse generators activates the internal clock generators, which control the DBL circuit and the sense amplifiers in order to accelerate a read operation.

Even though the DWL structure was adopted, the signal delay time of the word line increases in proportion to the chip size. Therefore, the memory array is divided into four mats. Each mat contains two blocks. Each block consists of four sections, each with 128 columns, 1024 rows, and eight redundancy rows. Only one section is activated at a time for power saving. Further, two row decoders were adopted to reduce the signal delay time of the word line. The main word line (MWL) runs through a mat and propagates the row decode signal. A section word-line (SWL) driver drives only 128 cells. The SWL drivers are arranged between every two sections, resulting in a total of 16 SWL drivers. Consequently, the signal delay time of the word line became half that of the conventional layout. Fig. 3 shows a photomicrograph of the 4-Mbit SRAM chip. The chip size is 7.46×17.41 mm^2 due to the compact layout design.

B. Dynamic Bit-Line Loads

The DBL circuit was developed to achieve high-speed bit-line precharge, equalization, and discharge during the initial stage of the read operation. A major asset of the

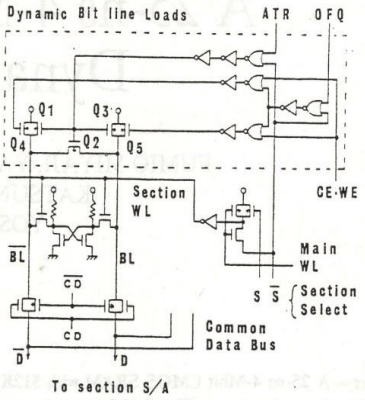

Fig. 4. DBL circuit.

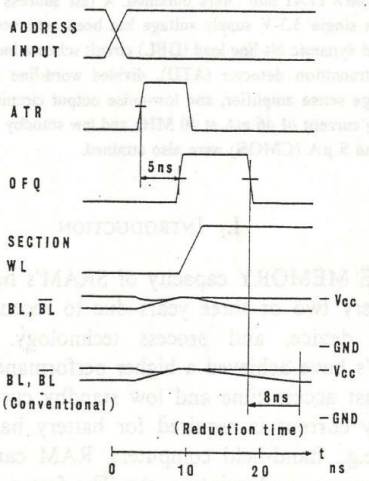

Fig. 5. Timing diagram for the read operation.

DBL circuit is that no special transistors, such as two kinds of NMOS transistors [1], are necessary to attain this function. As seen in Fig. 4, the DBL circuit consists of five PMOS transistors, five CMOS inverters, and four CMOS NOR gates. The control signal ($CE \cdot WE$) is at low level in the read operation and at high level in the write operation. Fig. 5 shows a timing diagram for the read operation. The timing relation between ATR and OFQ is shown in Fig. 5, and these pulses are generated by the internal clock generator. When an address transition occurs, the bit lines in a selected section are precharged and equalized to the V_{cc} level by the PMOS transistors $Q1$, $Q2$, and $Q3$ during the ATR pulse. Just before the ATR pulse goes low, the bit-line load PMOS transistors $Q4$ and $Q5$ are cut off by the OFQ pulse, which is delayed 5 ns from the positive edge of the ATR pulse. As the result of this operation, the bit-line load consists of only the stray capacitance. Successively, a selected SWL goes to the high level, and the memory cells are connected to the bit lines. Due to the small capacitance load on the bit line, the memory cell can rapidly drive the bit-line load. Therefore, the transition speed of the voltage difference in the bit-line pair ($BL - \overline{BL}$) is 8 ns faster than the conventional circuit in

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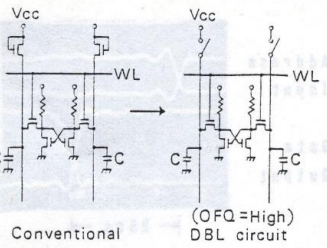

Fig. 6. Concept of DBL.

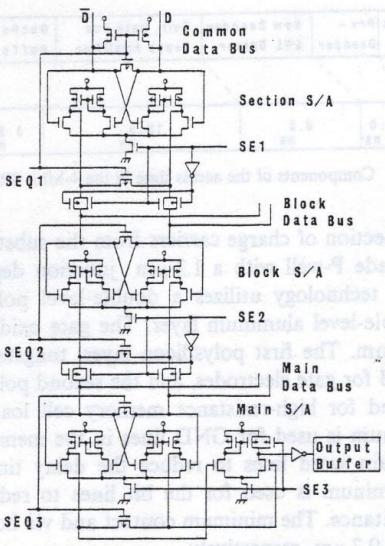

Fig. 7. Three-stage sense amplifier circuit.

which bit lines are connected through the normally-on NMOS transistors [4]. The concept of the DBL circuit is shown in Fig. 6. In the conventional circuit placed in the left part of Fig. 6, the bit-line loads consist of the NMOS transistor and the stray capacitance. On the other hand, the DBL circuit during the OFQ pulse is high level, and the bit-line load is only the stray capacitance. Therefore, the memory cell can rapidly drive the bit-line load, resulting in a fast access time.

C. Sense Amplifier

To attain high-speed data sense and transfer, a three-stage sense amplifier technique was adopted, as is shown in Fig. 7. A double-end current-mirror amplifier was applied for the sense amplifier because of its fast sense speed, large voltage gain, and good output voltage stability. For the first stage, section sense amplifiers were placed every 16 columns in each section. For the second stage, block sense amplifiers were placed every half-section in each block. For the third stage, main sense amplifiers were placed under block 1. These sense amplifiers are controlled by the control signals ($SE1$, $SE2$, and $SE3$), which are related to the column address signals.

An equalization technique is used for the common data buses, block data buses, main data buses, and all stages of the sense amplifier. Equalization is performed by the equalization pulses ($SEQ1$, $SEQ2$, and $SEQ3$), which are generated by the clock generator. This technique is indispensable not only to attain faster data transmission for every data pass but also to suppress incorrect data before the correct data appear in the sense amplifiers [6]. The obtained gains of the section sense amplifier, block sense amplifier, and main sense amplifier by using simulation (SPICE 2) were 2, 13, and 8, respectively. Therefore, the total gain of over 200 was attained. In this sense amplifier scheme, the block sense amplifier directly drives the main data bus through the transfer gates. Even though the signal is seriously delayed because of the large stray capacitances in the main data bus, the main sense amplifier rapidly amplifies the delayed signal. Due to the short data bus line on the output of the third sense amplifier, the sensed data are quickly transferred to the output circuit.

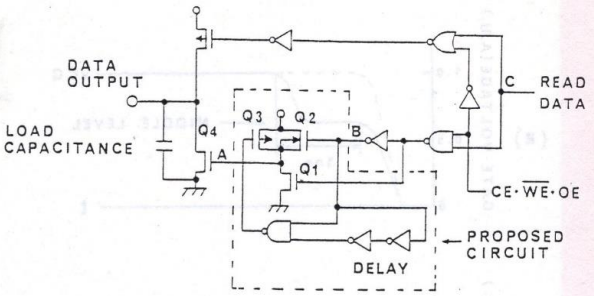

Fig. 8. Noise-reduction output circuit.

D. Output Circuit

The key issue for designing the high-speed SRAM with byte-wide organization is noise reduction. There are two kinds of noise: V_{cc} noise and GND noise. In the high-speed SRAM with byte-wide organization, when the output transistors drive a large load capacitance, the noise is generated and multiplied by 8 because eight outputs may change simultaneously. It is an especially serious problem for the data zero output. That is to say, when the output NMOS transistor drives the large load capacitance, the GND potential of the chip goes up because of the peak current and the parasitic inductance of the GND line. Therefore, the address buffer and the ATD circuit are influenced by the GND bounce, and unnecessary signals are generated. Due to the delay of the valid data, the access time becomes longer in the worst case. Therefore, the new two-step drive scheme was proposed, and good operation was confirmed.

Fig. 8 shows a proposed noise-reduction output circuit. The waveforms of the proposed and conventional output circuits are shown in Fig. 9. In the conventional circuit, nodes A and B are connected directly as shown in Fig. 8 (its operation and characteristics are shown by the dotted lines in Fig. 9). Due to the high-speed driving of transistor $Q4$, GND potential goes up, and the valid data are delayed by the output ringing.

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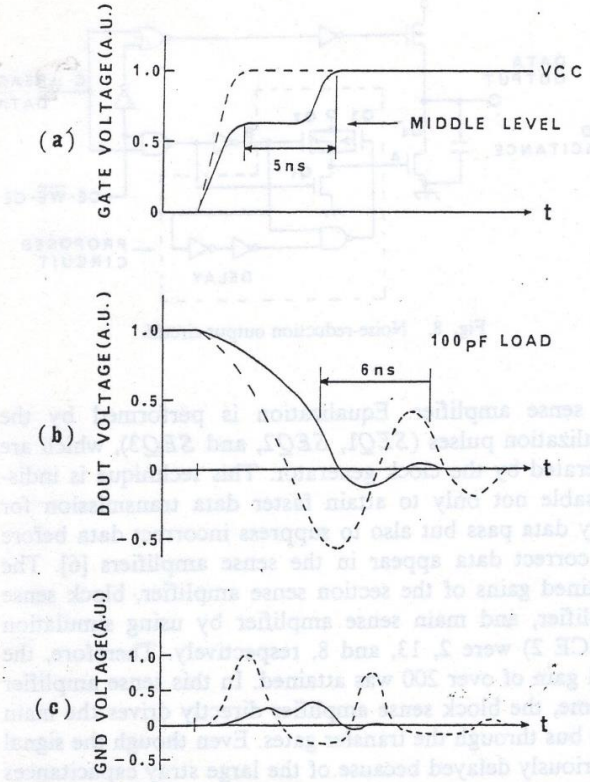

Fig. 9. Waveforms of proposed (solid line) and conventional (dotted line) output circuits: (a) gate bias, (b) data output, and (c) GND bounce.

On the other hand, the new noise-reduction output circuit consists of one PMOS transistor, two NMOS transistors, one NAND gate, and the delay part (its characteristics are shown by the solid lines in Fig. 9). The operation of this circuit is explained as follows. The control signal $(CE \cdot \overline{WE} \cdot OE)$ is at high level in read operation and low level in write operation. When the data zero output of logical high level is transferred to node C, transistor $Q1$ is cut off, and $Q2$ raises node A to the middle level. Therefore, the peak current that flows into the GND line through transistor $Q4$ is reduced less than one half that of the conventional circuit because $Q4$ is driven by the middle level. After a 5-ns delay counting from the beginning of the middle level, transistor $Q3$ raises node A to the V_{cc} level. As a result, the conductance of $Q4$ becomes maximum, but the peak current is small because of the low output voltage. Therefore, the increase of GND potential is small, and the output ringing does not appear. For example, when a 100-pF load capacitance is driven, the valid data appear approximately 6 ns faster than the valid data of the conventional circuit.

III. Process Technology

The 4-Mbit SRAM was fabricated using a 0.5-μm CMOS technology, which includes 0.5-μm channel-length LDD NMOS transistors and 0.6-μm channel-length LDD PMOS transistors. For low-temperature process and inhibition against collection of charge carriers from the substrate [8], the retrograde P-well with a 1.2-μm junction depth was used. This technology utilizes a double-level polysilicon and a double-level aluminum layer. The gate oxide thickness is 11 nm. The first polysilicon layer, tungsten polycide, is used for gate electrodes, and the second polysilicon layer is used for high-resistance memory cell loads. The first aluminum is used for GND lines in the memory cell and the main word lines to reduce the delay time. The second aluminum is used for the bit lines to reduce the stray capacitance. The minimum contact and via hole sizes are 0.6 and 0.7 μm, respectively.

The memory cell consists of four NMOS transistors and two high-resistance polysilicon loads, and the cell size is $3.6 \times 5.875\ \mu m^2$ [5].

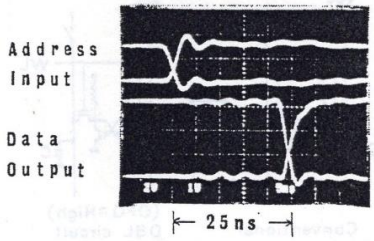

Fig. 10. Waveforms of the address access time.

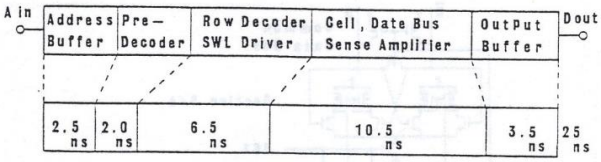

Fig. 11. Components of the access time in the 4-Mbit SRAM.

IV. RAM Performance

Fig. 10 shows the output waveforms of the address access time. A typical address access time of 25 ns has been attained with a 30-pF load capacitance and a single 3.3-V supply voltage at 25°C. Fig. 11 shows the components of the access time for the circuit blocks in the 4-Mbit SRAM. The delay time from an address input to a predecoder output is 4.5 ns, from a predecoder output to a word line it is 6.5 ns, from a word line to a sense amplifier output it is 10.5 ns, and from the sense amplifier output to a data output it is 3.5 ns. Typical operating currents of 33 and 46 mA have been obtained at 10 and 40 MHz, respectively. Standby currents of 70 and 5 μA have been realized at TTL input levels and CMOS input levels, respectively.

The chip measures $7.46 \times 17.41\ mm^2$. The memory cells occupied 68.3 percent in the chip area due to the compact layout in the peripheral circuit. Fig. 12 shows the 4-Mbit SRAM assembled into a standard ceramic 32-pin 400-mil dual-in-line package. The RAM contains eight spare rows that can independently replace eight defective rows in each

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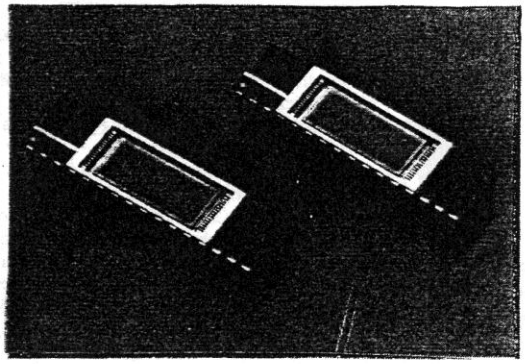

Fig. 12. 4-Mbit SRAM assembled into a 400-mil DIP.

TABLE I
TYPICAL CHARACTERISTICS

Organization	512KW x 8bit
Chip size	7.46 x 17.41 mm²
Cell size	3.6 x 5.875 um²
Power supply	3.3V
Address access time	25ns
Active current	33mA at 10MHz
	46mA at 40MHz
Standby current	70uA at VIH=2.2V
Package	32Pin. 400mil DIP
Redundancy	8 rows

mat with the laser-fuse blowing technique. The typical characteristics of the 4-Mbit SRAM are listed in Table I.

V. CONCLUSION

A 4-Mbit CMOS SRAM with 512K word × 8-bit organization has been designed and fabricated using 0.5-μm double-polysilicon and double-aluminum retrograde P-well CMOS technology. These advanced process technologies and compact layout design have realized a cell size of $3.6 \times 5.875\ \mu m^2$ and a chip size of $7.46 \times 17.41\ mm^2$. New circuit techniques were developed to achieve high performance in speed. The four-mat division, two-row decoder, dynamic bit-line load circuit, three-stage sense amplifier, and noise-reduction output circuit have achieved a typical access time of 25 ns. A low operating current of 46 mA at 40 MHz and low standby currents of 70 μA (TTL) and 5 μA (CMOS) have also been attained.

ACKNOWLEDGMENT

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Mr. Miyaji is a member of the Institute of Electronics, Information and Communication Engineers of Japan.

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Sony's 25 nano sec access time world-fastest 4MSRAM CMOS chip used the dynamic bit-line (DBL) scheme normally used only in the conventional DRAM chips. The idea of using the DBL circuit for this SRAM chips was proposed by Fumio Miyaji and his idea made the world fastest access time SRAM chip which is an essential part for realizing the SNAPSHOT digital image acquisition system of digital still pictures for modern consumer digital camera applications.

Fumio Miyaji was born in Hamamatsu, Japan, on July 23, 1954. He received the B.S. degree in electrical engineering from Mie University, Tsu, Japan, in 1978.

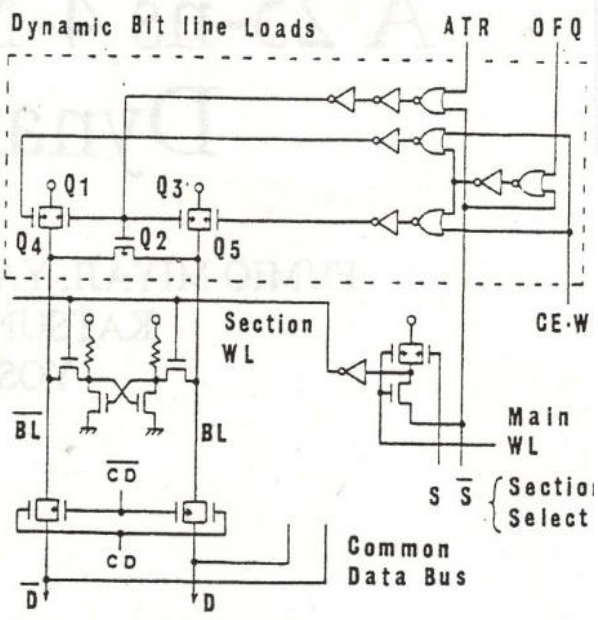

Fig. 4. DBL circuit.

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